

IN THE CLAIMS

1. (Original) A monolithically integrated amplifier comprising:

a heterojunction bipolar transistor (HBT) comprising a contact epitaxial layer; and

a field effect transistor (FET) configured to current-limit a current to the HBT, the FET comprising a portion of the contact epitaxial layer.
2. (Original) The monolithically integrated amplifier of claim 1 wherein the FET is configured to current-limit a base current to the HBT.
3. (Original) The monolithically integrated amplifier of claim 2 wherein the FET is un-gated.
4. (Original) The monolithically integrated amplifier of claim 2 wherein the FET is gated.
5. (Original) The monolithically integrated amplifier of claim 2 wherein a source of the FET is in electrical communication with a gate of the FET through a source resistor.
6. (Original) The monolithically integrated amplifier of claim 2 wherein a channel width of the FET is selected to limit the base current to less than I_{Bsat} where $I_{Bsat} < 2 * I_{Bnom}$ where I_{Bnom} is a nominal base current.
7. (Original) The monolithically integrated amplifier of claim 6 wherein the channel width of the FET is selected such that $I_{Bsat} > I_{Bnom}$.
8. (Original) The monolithically integrated amplifier of claim 1 wherein the FET is configured to current-limit a collector current to the HBT.
9. (Original) The monolithically integrated amplifier of claim 8 wherein the FET is un-gated.

10. (Original) The monolithically integrated amplifier of claim 8 wherein the FET is gated.
11. (Original) The monolithically integrated amplifier of claim 8 further comprising a source resistor electrically connecting a source of the FET to a gate of the FET.
12. (Original) The monolithically integrated amplifier of claim 1 wherein the FET is configured in series with an RF connection to a collector of the HBT.
13. (Original) The monolithically integrated amplifier of claim 12 wherein the FET is ungated.
14. (Original) The monolithically integrated amplifier of claim 12 wherein the FET is gated.
15. (Original) The monolithically integrated amplifier of claim 12 further comprising a source resistor connecting a source of the FET to a gate of the FET.
16. (Original) The monolithically integrated amplifier of claim 1 wherein the FET is selected from a group comprising MOSFET, MESFET, pHEMT and HEMT.
17. (Original) A monolithically integrated amplifier comprising:
 - a heterojunction bipolar transistor (HBT) comprising at least one HBT cell, the HBT cell comprising a contact epitaxial layer; and
 - a field effect transistor (FET) configured to current-limit a current to the at least one HBT cell, the FET comprising a portion of the contact epitaxial layer.
18. (Original) The monolithically integrated amplifier of claim 17 wherein the FET is configured to current-limit a base current to the at least one HBT cell.
19. (Original) The monolithically integrated amplifier of claim 17 wherein the FET is configured to current-limit a collector current to the at least one HBT cell.

20. (Original) The monolithically integrated amplifier of claim 17 wherein the FET is configured in series with an RF connection to a collector of the at least one HBT cell.
21. (Original) The monolithically integrated amplifier of claim 17 further comprising a source resistor connecting a gate of the FET to a source of the FET.
22. (Original) A method for protecting an amplifier comprising a heterojunction bipolar transistor by providing a monolithically integrated field effect transistor to limit the current flowing through the heterojunction bipolar transistor to a predetermined current, wherein the monolithically integrated field effect transistor behaves substantially as a resistor during normal operation of the amplifier.
23. (Original) The method of claim 22 wherein the monolithically integrated field effect transistor reduces a variation of output power to a change in load phase.
24. (Original) The method of claim 22 further comprising biasing a gate voltage of the field effect transistor negatively with respect to a source voltage of the field effect transistor such that the negatively biased gate voltage depends at least in part on a current through the field effect transistor.
25. (Original) A method for reducing collector current variations to a change in load phase in an amplifier comprising a heterojunction bipolar transistor, the method comprising the steps of: providing a monolithically integrated field effect transistor to limit the current flowing through the heterojunction bipolar transistor to a predetermined current, wherein the monolithically integrated field effect transistor behaves substantially as a resistor during normal operation of the amplifier.